SEMICONDUCTOR DEVICE

Background of the Invention

Field of the Invention

The present invention relates to a semiconductor device, and more particularly to a semiconductor device that comprises a resistor film consisting of polysilicon formed in an insulating film on a semiconductor substrate.

Background Art

Fig. 5 is a sectional view showing a schematic configuration of a conventional integrated circuit that comprises polysilicon resistors. In this drawing, reference numeral 1 is a silicon substrate, i.e. a semiconductor substrate; 2 is an insulating film consisting of a field oxide film or an interlayer insulating film formed on the silicon substrate 1, 3 is a resistor film consisting of polysilicon formed in the insulating film 2; 4A and 4B are terminal wirings of the resistor film 3 formed on the insulating film 2, and connected to the resistor film 3 through connecting portions 5A and 5B.

The integrated circuit comprising a conventional resistor film is constituted as described above, and heat generated in the resistor film 3 is dissipated into the silicon substrate 1

through the insulating film 2 underneath the resistor film 3, but the heat is not sufficiently transferred because the insulating film 2 underneath the resistor film 3 is as thick as about 0.5 μm, thereby raising a problem of low resistance to instantaneous surge electric power.

Specifically, as shown by curve a in Fig. 3 that indicates the result of simulation of the temperature rise of the resistor film 3 in the case where a step electric power of about 3 mW was consumed, a temperature rise per unit power consumption was as large as 2,200 deg./W, in 1 μs showing a large transient heat impedance.

Also, as shown by curve a in Fig. 4 that indicates the result of ESD (electrostatic discharge) simulation of discharge from a 200 pF capacitor, temperature rose rapidly in 700 ns after starting power supply to over 2,000 K, leading to thermal breakdown.

In recent years, since the resistor film 3 is becoming thinner accompanying the size reduction of transistors due to the advancement of micromachining technology, the resistance to surge power tends to further lower.

Summary of the Invention

Therefore, an object of the present invention is to cope with such a problem, and to provide a semiconductor device that

can improve a resistance to a surge power of integrated circuits or the like having resistor films.

According to one aspect of the present invention, a semiconductor device comprises a semiconductor substrate, a first insulating film formed on the semiconductor substrate, a polysilicon resistor film formed on the first insulating film, a second insulating film formed on the resistor film, a high heat conductor film consisting of a highly heat-conducting material formed on the second insulating film, and a pair of terminal wirings formed on the second insulating film and connected to the resistor film, wherein a thickness of the second insulating film is thinner than a thickness of the resistor film.

According to another aspect of the present invention, a semiconductor device comprises a semiconductor substrate, a first insulating film formed on the semiconductor substrate, a polysilicon resistor film formed on the first insulating film, a second insulating film formed on the resistor film, a high heat conductor film consisting of a highly heat-conducting material formed on the second insulating film, and a pair of terminal wirings formed on the second insulating film and connected to the resistor film, wherein a thickness of the high heat conductor film is thicker than a thickness of the resistor film.

According to the present invention, the resistance to instantaneous surge power of the semiconductor devices having

resistor films can be improved.

Other and further objects, features and advantages of the invention will appear more fully from the following description.

Brief Description of the Drawings

Fig. 1 is a sectional view showing a schematic constitution of Embodiment 1.

Fig. 2 is a top view showing a schematic constitution of modification of Embodiment 1.

Figs. 3 is a graph of characteristic curves showing the results of a temperature rise simulation obtained to clarify the constitution of Embodiment 1 as well as to confirm the effect

Figs. 4 is a graph of characteristic curves showing the results of an ESD simulation obtained to clarify the constitution of Embodiment 1 as well as to confirm the effect

Fig. 5 is a sectional view showing a schematic configuration of a conventional integrated circuit that comprises polysilicon resistors.

Detailed Description of the Preferred Embodiments

Embodiment 1

Embodiment 1 of the present invention will be described below referring to the drawings.

Fig. 1 is a sectional view showing a schematic constitution of Embodiment 1. In Fig. 1, reference numeral 1 is a silicon substrate, i.e. a semiconductor substrate; 2 is an insulating film consisting of a field oxide film or an interlayer insulating film formed on the silicon substrate 1; 3 is a resistor film consisting of polysilicon formed in the insulating film 2; 4A and 4B are terminal wirings of the resistor film 3 formed on the insulating film 2, and connected to the resistor film 3 through connecting portions 5A and 5B.

Reference numeral 6 denotes a high heat conductor film consisting of a high heat conductor material formed above the resistor film 3 through a thin insulating film 2A, and is made of aluminum (Al) or an alloy thereof.

T1 is a thickness of the insulating film 2 (silicon oxide film) provided underneath the resistor film 3, for example 0.5 μm. T2 is the thickness of the resistor film 3, for example 0.15 μm. T3 is a thickness of the insulating film 2A (silicon oxide film) between the resistor film 3 and the high heat conductor film 6. T4 is a thickness of the high heat conductor film 6. Specific values of T3 and T4 will be described later.

Embodiment 1 is constituted as described above. Thereby, since a heat path is produced from the resistor film 3 to the high heat conductor film 6 through the thin insulating film 2A over the resistor film 3, in addition to a path for dissipating

heat into the silicon substrate 1 through the thin insulating film 2 underneath the resistor film 3, a heat capacity of the high heat conductor film 6 can temporarily absorb the heat generated in the resistor film 3 due to surge power until the heat is accumulated in the high heat conductor film 6, thus improving the resistance to the surge power.

In this case, since the pulse width of the surge current is usually about 0.2 μs, the heat generated in the resistor film 3 passes through the insulating film 2A in about the above-described time and reaches the high heat conductor film 6. Furthermore, in order to maintain the heat absorption by the high heat conductor film 6 thereafter, a thickness T3 of the insulating film 2A becomes an important factor.

Similarly as an interlayer film used in general IC processes, when the thickness T3 of the insulating film 2A is, for example, 0.5μm, the time for heat to pass is about 1 μs. Therefore, the thickness is too thick for a pulse width of the above-described surge current to expect sufficient effect.

Also, since the heat transferred to the high heat conductor film 6 scarcely diffuses to a lateral direction because of the narrow pulse width of a surge current, a heat absorption must be supplemented by increase in thickness.

Figs. 3 and 4 are graphs of characteristic curves showing the results of a temperature rise simulation and an ESD simulation

obtained to clarify the constitution of Embodiment 1 as well as to confirm the effect, and show characteristics of each of T3 and T4 when the thicknesses of T3 and T4 is set to various values in the structure shown in Fig. 1, for example, T1 = 0.5 μm and T2 = 0.15 μm. That is, in these characteristic diagrams, a curve b shows when T4 = 1 μm and T3 = 0.2 μm, a curve c shows when T4 = 0.2 μm and T3 = 0.1 μm, a curve d shows when T4 = 0.45 μm and T3 = 0.1 μm, and a curve e shows when T4 = 1 μm and T3 = 0.1 μm.

As seen in the curves c, d, and e of Fig. 4, when the thickness T3 of the insulating film 2A on an upper surface of the resistor film is T3 = 0.1 μm, thinner than the thickness T2 = 0.15 μm of the resistor film 3, a peak temperature lowers to 1,400 K., then the permanent breakdown does not occur. However, as seen in the curve b, when the thickness T3 = 0.2 μm, thicker than the thickness of the resistor film 3, a temperature rises rapidly causing permanent breakdown, and it is seen that a resistance to surge power is low.

For the thickness T4 of Al of the high heat conductor film 6, when T4 = 0.2 μm or more, thicker than the thickness of the resistor film 3, permanent breakdown does not occur, as seen in any of curve c (T4 = 0.2 μm), curve d (T4 = 0.45 μm), and curve e (T4 = 1 μm).

When the curves c, d, and e are compared, the peak temperature of the curve d or curve e where the thickness T4 of Al is twice

the thickness T2 of the resistor film 3 or more, 0.45 μm or 1 μm, respectively, is nearly 200 K lower than a peak temperature of the curve c, achieving larger effect. Furthermore, when transient heat impedance characteristics in the above-described cases are viewed from Fig. 3, an instantaneous temperature rise up to 0.4 μs is large in the curve b and the curve a (prior art) in Fig. 4, which lead to permanent breakdown, and it is seen that characteristics up to this time point are significantly related to the occurrence of ESD breakdown.

From the above results, in Embodiment 1, it was concluded, to obtain the sufficient effect of absorbing surge power, that the thickness T3 of the insulating film 2A should be thinner than the thickness T2 of the resistor film 3, and the thickness T4 of the high heat conductor layer 6 should be thicker than T2, preferably twice T2 or more.

Although the high heat conductor layer 6 is composed of Al or the alloys thereof, the materials are not limited to these, and the same effect can be expected from copper, poly-amorphous silicon, or the like. The same effect can also be expected from a multi-layer wiring structure in which a wiring layer is further provided on the high heat conductor layer 6 through an insulating film.

Furthermore, heat capacity can further be increased by making the high heat conductor layer 6 wider than the resistor film 3, not only to cover the resistor film 3, as shown in Fig. 2. Also, when the high heat conductor layer 6 is used in common with terminal wirings 4A and 4B made of Al or the like, since the area of the high heat conductor layer 6 can be increased by using the high heat conductor layer 6 as a part of the ground/power wiring region or input/output pads, the resistance to surge power of not only an extremely short time such as ESD, but also a relatively long time of the millisecond order, can be improved.

Since the semiconductor device according to the present invention is constituted as described above, the resistance to instantaneous surge power of the semiconductor devices having resistor films can be improved.

The entire disclosure of a Japanese Patent Application No. 2000-377581, filed on December 12, 2000 including specification, claims, drawings and summary, on which the Convention priority of the present application is based, are incorporated herein by reference in its entirety.